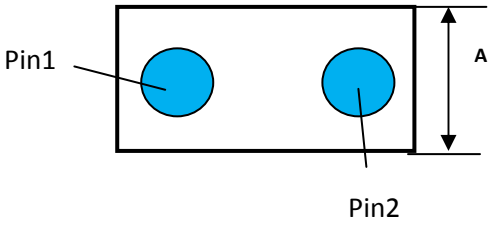
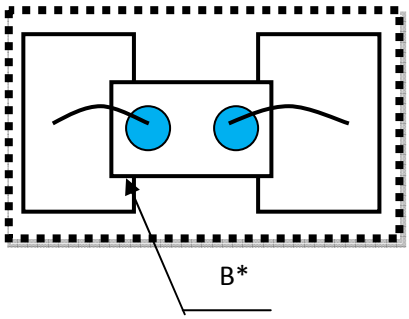
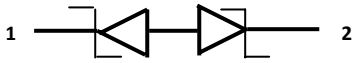
Mechanical data: A_x= 450um. A_y=330um.
Chip thickness : a) KS-05V2M1A 138+/-12um
Back side: Ti-Ni-Ag;
b) KS-05V2M1B without grinding 470+/-20um
Back side: without metallization.
Top Metal: Al- for wire bonding. Pad Size Pin 1, 2 - ø85 um.







Bonding diagram in DFN-2L

B* - the thickness of the dielectric between the crystal and the frame should be greater then 10 um

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Working Peak Reverse Voltage	V_{RWM}		5,0.	V
Peak Pulse Power	P_{pp}	t_p= 8/20uS	45*	W
Peak Pulse Current	I_{pp}	t_p= 8/20uS	3,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	+/-8,0 (Contact);	kV
Max.junction temperature	T_j		+150	ºC

Characteristics .Ta=25ºC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Diode reverse leakage current.	V=±5,0 V	-	-	0,9	uA
V_{BR}	Breakdown voltage.	I_R=1mA	6,4	-	9,0	V
C_j	Diode capacitance. Pin 1 to 2.	F=1MHz, V_{dc}=0 V.	-	0,35	0,4	pF
V_{CL}	Clamping voltage	I_{pp}=1,0A; I_{pp}= 3,0A; t_p= 8/20uS .	- -	- -	12,0* 15,0*	V

*- For Device testing.