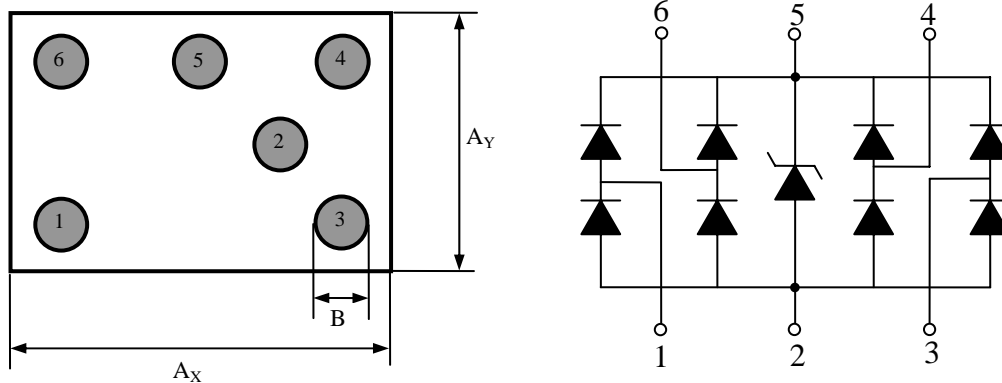


Chip for dual USB 2.0 Integrated ESD protection to IEC 61000-4-2 level 4.



Mechanical date: $A_x=800\mu\text{m}$, $A_y=580\mu\text{m}$, $B=90\mu\text{m}$

Chip thickness: $230\pm 20\mu\text{m}$

Scribe Line width - $60\mu\text{m}$.

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
DC input voltage range	$V_{I/O}$	-	+5.5 max	V
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	± 8.0 (Contact)	kV
Max. junction temperature	T_j	-	+125	$^{\circ}\text{C}$

Characteristics ($T_j=25^{\circ}\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{lkg}	Diode reverse leakage current. Pins 1, 3, 4, 6 to ground	$V=+3,0\text{ V}$	-	-	100	nA
V_{BR}	Zener diode breakdown voltage. Pin 5 to 2.	$I_Z=1\text{mA}$	6,1	7,0	8,5	V
C_z	Zener diode capacitance to ground. Pin 5 to 2.	$F=1\text{MHz}$, $V_{dc}=0\text{ V}$. Pin 5 = +3,0 V	-	40	-	pF
V_F	Forward voltage	$I_F=1\text{mA}$	-	0,7	-	V
$C_{I/O}$	Pin capacitance to ground. Pins 1, 3, 4, 6 to 2.	$V_{dc}=0\text{ V}$; $f=1\text{MHz}$. Pin 5 = +3,0 V	-	1,0	-	pF

*- For Device testing