



**Mechanical data:**  $A_x= 800\mu\text{m}$ ,  $A_y=580\mu\text{m}$ ,  $B=90\mu\text{m}$

**Chip thickness:** a)  $203\pm 12\mu\text{m}$ .

c) by agreement with the customer

d) without grinding  $460\pm 20\mu\text{m}$

**Scribe Line width** -60 $\mu\text{m}$ .

**Top Metal:** Al – thickness  $4,0\pm 0,4\mu\text{m}$ ;

**Back side** – Ti-Ni-Ag– thickness 0,1-0,3-0,5 $\mu\text{m}$  or without metallization

**Probing:** a) sampling testing : no bad dice inking, guaranteed good dice quantity  $\geq 93\%$

b) 100% testing (if agreed with customer): wafer mapping data, no bad dice inking

**Schematic and pinning diagram.**

Pin#	Description
1, 3, 4,6	I/O-Lines
5	Vcc
2	GND

### Limiting values

Parameter	Symbol	Conditions	Value	Unit
DC input voltage range	$V_{I/O}$	-	+5.5max	V
Peak Pulse Power	$P_{pp}$	$t_p = 8/20\mu\text{s}$	55	W
Peak Pulse Current	$I_{pp}$	$t_p = 8/20\mu\text{s}$	4,0	A
Electrostatic Discharge	$V_{ESD}$	IEC 61000-4-2, level4.	$\pm 9.0$ (Contact)	kV
Max. junction temperature	$T_j$	-	+125	$^{\circ}\text{C}$

### Characteristics( $T_j=25^{\circ}\text{C}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{lkg}$	Diode reverses leakage current. Pins 1, 3, 4, 6 to Pin 2.	$V=+5,0\text{V}$	-	-	0,2	$\mu\text{A}$
$V_{BR}$	Zener diode breakdown voltage. Pin 5 to 2.	$I_Z=1\text{mA}$	6,1	7,0	8,0	V
$V_F$	Forward voltage. Pin2 to Pin5.	$I_F=1\text{mA}$	-	0,7	-	V
$V_{cl}^*$	Clamping Voltage	$I_{pp}=1\text{A}, t=8/20\mu\text{s};$ $I_{pp}=4\text{A}, t=8/20\mu\text{s}$	-	-	10,0 13,0	V
$C_{I/O}$	Pin capacitance. Pins 1, 3, 4, 6 to Pin2.	$V_{dc}=0\text{V}; f=1\text{MHz}.$	-	0,65	0,8	pF
$C_{I/O-I/O}$	Any I/O pin to I/O.	$V_{dc}=0\text{V}; f=1\text{MHz}.$	-	0,3	-	pF

\*- For Device testing