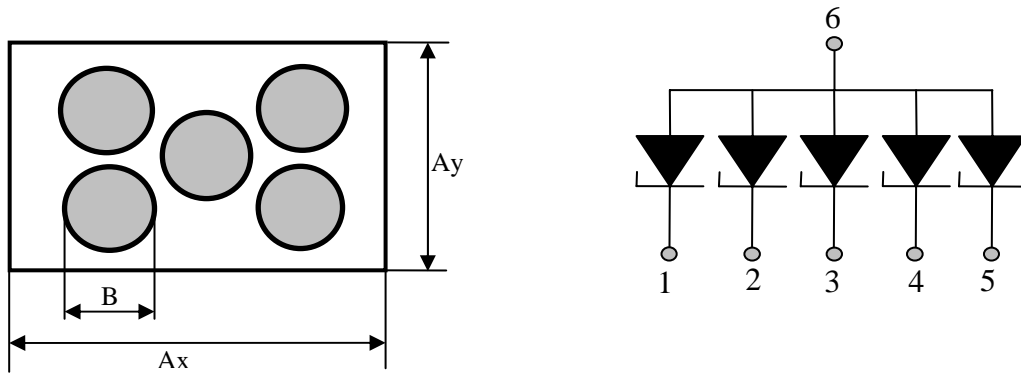


Rev.1. March 2010.

KS-3,3V5

Chip low capacitance 5- fold ESD protection diode.



Mechanical date: $A_x=590\mu\text{m}$, $A_y=450\mu\text{m}$
 $B=100\mu\text{m}$

Schematic and pinning diagram.

Chip thickness: $138\pm 12\ \mu\text{m}$

Scribe Line width - $60\mu\text{m}$.

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	3,3	V
Peak Pulse Power	P_{pp}	$t_p=8/20\mu\text{s}$	40*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{s}$	3,5*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	$I_R=1\text{mA}$	5,3	5,7	5,9	V
I_R	Reverse leakage current	$V=3,3\text{V}$	-	80	250	nA
V_{CL}	Clamping Voltage	$I_{pp}=1.0\text{A}$, $t_p=8/20\mu\text{s}$ $I_{pp}=2.5\text{A}$, $t_p=8/20\mu\text{s}$ $I_{pp}=3.5\text{A}$, $t_p=8/20\mu\text{s}$	-	-	9* 11* 12*	V
C_J	Diode capacitance	$V_R=0\ \text{V}$, $f=1\text{MHz}$	-	30	40	pF

*- For Device testing