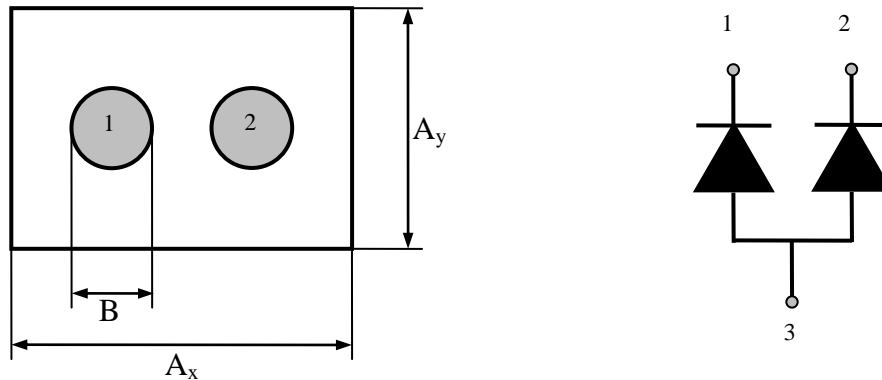


Rev.1. March 2010.

KS-5,0V2

Chip low capacitance 2- fold ESD protection diode.



Mechanical date: $A_x = 340\mu\text{m}$, $A_y = 240\mu\text{m}$, $B = 80\mu\text{m}$
Chip thickness: $138 \pm 12\ \mu\text{m}$
Scribe Line width - $60\mu\text{m}$.
Top Metal: Al - for wire bonding.
Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,0	V
Peak Pulse Power	P_{pp}	$t_p = 8/20\mu\text{s}$	25*	W
Peak Pulse Current	I_{pp}	$t_p = 8/20\mu\text{s}$	2,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>15 (Contact); >20 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j = 25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	$I_R = 1\text{mA}$	6,05	-	7,1	V
I_R	Reverse leakage current	$V = 5\text{V}$	-	-	0,2	μA
V_{CL}	Clamping Voltage	$I_{pp} = 2,0\text{A}$, $t_p = 8/20\mu\text{s}$	-	-	12,5*	V
V_f	Forward Voltage	$I_f = 10\text{mA}$	-	-	1,1	
C_j	Diode capacitance	$V_R = 0\ \text{V}$, $f = 1\text{MHz}$	-	-	9,5	pF

*- For Device testing