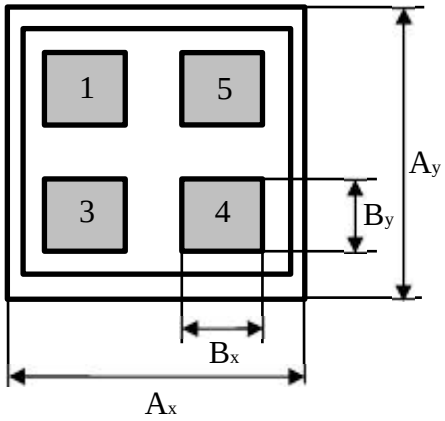
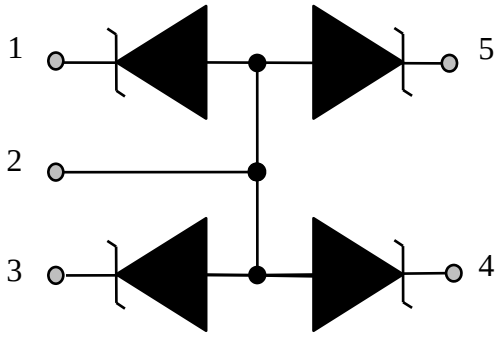
VSP-MIKRON

Rev.1. March 2010.

KS-5,0V4L1

Chip low capacitance 4- fold ESD protection diode.





Mechanical date: $A_x=A_y=340um$. $B_x=B_y=70um$

Schematic and pinning diagram.

Chip thickness: 230+/-20um

Scribe Line width - 60um.

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,0	V
Peak Pulse Power	P_{pp}	t_p=8/20us	25*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	2,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15(Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Reverse leakage current	V=3,0V	-	-	0,9	uA
V_{BR}	Breakdown voltage	I_R=1uA	6,15	-	7,15	V
C_J	Diode capacitance	F =1MHz, V_R=3,0V	-	-	9,5	pF
R_{diff}	Differential resistance	I_R=15A, t_p=2,5us	-	-	1,1*	Ohm

*- For Device testing