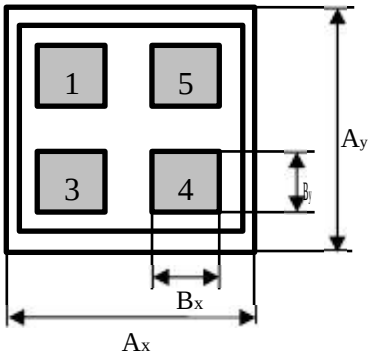
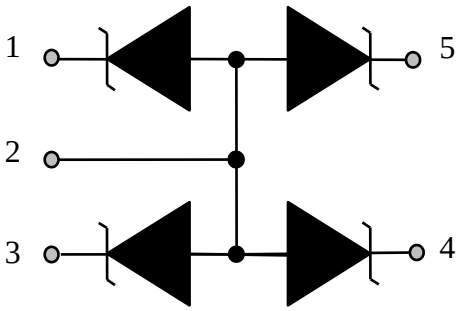
VSP-MIKRON

Rev.1. March 2010.

KS-5,0V4L2

Chip low capacitance 4- fold ESD protection diode.





Mechanical date: A_x=A_y=750um.
B_x=B_y= 160um
Chip thickness: 230+/-20um
Scribe Line width - 60um.
Top Metal: Al - for wire bonding.
Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,0	V
Non-repetitive reverse pulse power dissipation	P_P	Square pulse t_p=1mS	24*	W
Non-repetitive peak pulse current	I_p	Square pulse t_p=1mS	2,66*	A
Peak Pulse Power	P_{pp}	t_p=8/20us	150*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	15*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15(Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Reverse leakage current	V=5,0V	-	-	0,65	uA
V_{BR}	Breakdown voltage	I_R=1mA	5,9	6,2	6,5	V
C_J	Diode capacitance	F =1MHz, V_R=0V F =1MHz, V_R=4V	-	-	200 110	pF
R_{diff}	Differential resistance	I_R=1,0mA	-	-	300*	Ohm
V_F	Forward voltage	I_F=200mA	-	-	1,25	V
V_{ZSM}	Non-repetitive peak reverse voltage	I_{ZSM}=2,66A, t_p=1mS	-	-	9*	V
V_{CL}	Clamping voltage	IR=15A, t_p=8/20uS	-	-	12*	V

*- For Device testing