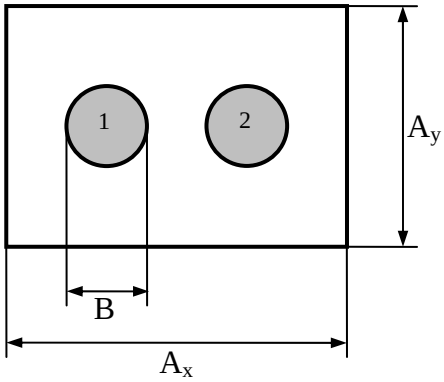
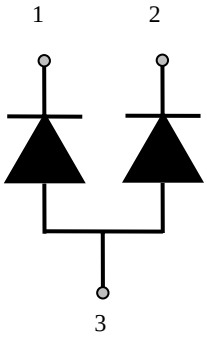
VSP-MIKRON

Rev.1. March 2010.

KS-5,0V2

Chip low capacitance 2- fold ESD protection diode.





Mechanical date: A_x= 340um, A_y=240um., B=80um
Chip thickness: 138+/-12 um
Scribe Line width - 60um.
Top Metal: Al - for wire bonding.
Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,0	V
Peak Pulse Power	P_{pp}	t_p=8/20us	25*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	2,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>15 (Contact); >20 (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=1mA	6,05	-	7,1	V
I_R	Reverse leakage current	V=5V	-		0,2	uA
V_{CL}	Clamping Voltage	I_{pp}=2,0A, t_p=8/20us	-	-	12,5*	V
V_f	Forward Voltage	I_f=10mA			1,1	
C_J	Diode capacitance	V_R=0 V, f =1MHz	-		9,5	pF

*- For Device testing