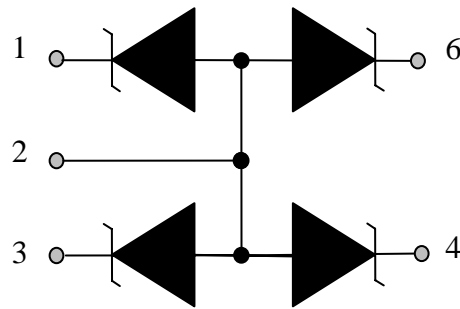
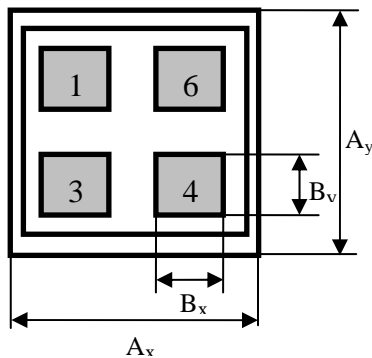


KS-5,0V4L2

Chip low capacitance 4- fold ESD protection diode.



Mechanical date: $A_x=A_y=750\mu\text{m}$.
 $B_x=B_y=160\mu\text{m}$

Chip thickness: $230\pm 20\mu\text{m}$

Scribe Line width - $60\mu\text{m}$.

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,0	V
Non-repetitive reverse pulse power dissipation	P_P	Square pulse $t_p=1\text{mS}$	24*	W
Non-repetitive peak pulse current	I_p	Square pulse $t_p=1\text{mS}$	2,66*	A
Peak Pulse Power	P_{pp}	$t_p=8/20\mu\text{s}$	150*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{s}$	15*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15(Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Reverse leakage current	$V=5,0\text{V}$	-	-	0,65	μA
V_{BR}	Breakdown voltage	$I_R=1\text{mA}$	5,9	6,2	6,5	V
C_J	Diode capacitance	$F=1\text{MHz}, V_R=0\text{V}$ $F=1\text{MHz}, V_R=4\text{V}$	-	-	200 110	pF
R_{diff}	Differential resistance	$I_R=1,0\text{mA}$	-	-	300*	Ohm
V_F	Forward voltage	$I_F=200\text{mA}$	-	-	1,25	V
V_{ZSM}	Non-repetitive peak reverse voltage	$I_{ZSM}=2,66\text{A}, t_p=1\text{mS}$	-	-	9*	V
V_{CL}	Clamping voltage	$I_R=15\text{A}, t_p=8/20\mu\text{S}$	-	-	12*	V

*- For Device testing