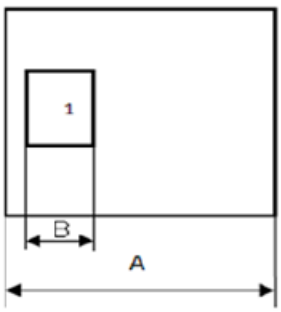

Mechanical data: A_x= 330 um, A_y=260um, B_x=B_y=85 um

Schematic and pinning diagram

Chip thickness: a) 138+/-12um on 4" wafer – for KSR-5.0V1U1A .
b) 470+/-20 um on 4" wafer – for KSR-5.0V1U1B.
c) 655+/-20um on 6" wafer – for KSR-5.0V1U1C.

Scribe Line width - 50um.

Top Metal - Pin 1: Al - for wire bonding.

Back side – Pin 2: a) Ti-Ni-Ag for soldering – for KSR-5.0V1U1A .
b) without metallization – for KSR-5.0V1U1B.
c) without metallization – for KSR-5.0V1U1C.

Probing:a)sampling testing: no bad dice inking guaranteed good dice quantity≥93%
b) 100% testing (if agreed with customer): wafer mapping data no bad dice inking

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	tp=8/20us	42*	W
Peak Pulse Current	I_{pp}	tp=8/20us	3*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	Tj	-	+150	ºC

Characteristics **(Ta=25ºC)**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=1mA	6,0	7,0	-	V
I_R	Reverse leakage current	V=±5V	-		0,9	uA
V_{CL}	Clamping Voltage	I_{pp}=1.0A, t_p=8/20us I_{pp}=3.0A, t_p=8/20us	-	-	10* 14*	V
C_J	Capacitance.	V_R=0 V, f =1MHz	-	0,6	0,8	pF

*- For Device testing