



Schematic and pinning diagram

Mechanical data: $A_x=380$, $A_y=420\mu\text{m}$

Pad Size: for Pin 1, 2 - $80 * 90 \mu\text{m}$;
 for Pin 3 - $140 * 100 \mu\text{m}$;
 Pin 4 – back side – GND.

Chip thickness: $675 \pm 20\mu\text{m}$.

Scribe Line width - $40\mu\text{m}$.

Top Metal: Al - for wire bonding.

Back side: Without metallization.

Probing: sampling testing: no bad dice inking; guaranteed good dice quantity $\geq 93\%$.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	$t_p= 8/20\mu\text{s}$	80*	W
Peak Pulse Current	I_{pp}	$t_p= 8/20\mu\text{s}$	4*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4. Contact and Air	>8 (Contact); >15 (Air).	kV
Max.junction temperature	T_j		+125	$^{\circ}\text{C}$

Characteristics ($T_a=25^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Breakdown voltage	V_{BR}	$I_R=1\text{mA}$. Pin3 to Pin4.	6,1	7,8	8,5	V
Reverse leakage current	I_R	$V=5\text{V}$. Pin 1,2,3 to Pin4	-	-	0,9	μA
Forward voltage	V_F	$I_F=15\text{mA}$. Pin4 to Pin1,2,3	-	-	1,15	V
Clamping Voltage. Pin 1,2 to Pin4	V_{CL}	$I_{pp}=1.0\text{A}$, $t_p=8/20\mu\text{s}$. $I_{pp}=4,0\text{A}$, $t_p=8/20\mu\text{s}$	-	-	12* 20*	V
Capacitance. Any I/O pin to Ground	C_j	$f=1\text{MHz}$, $V_{dc}=0\text{V}$.	-	0,6	0,8	pF
Capacitance between I/O pins.	C_j	$f=1\text{MHz}$, $V_{dc}=0\text{V}$.	-	0,3	0,4	pF

*-For Device testing