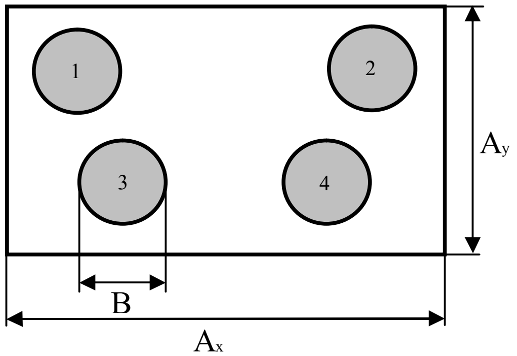
VSP-MIKRON

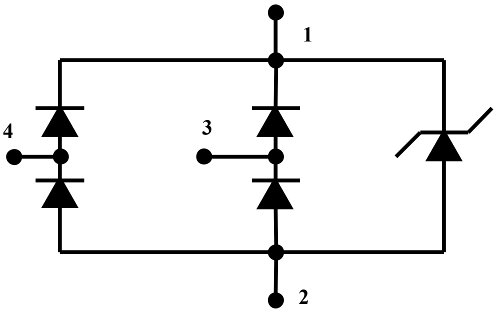
RoHS

Rev.4. March 2014. Preliminary

KSR-5.0V2M1

Chip for Low Capacitance 2-Line ESD protection in wafer form, 4 inch.





Mechanical data: A_x=630um, A_y=330um, B=80um

Schematic and pinning diagram.

Thickness: a)138+/-12um; b) max.450um without grinding.
Scribe Line width - 60um.
Top Metal: Al - for wire bonding, d=4.0+/-0.4 um.
Back Metal: a) Ti-Ni-Ag; b) without metallization.
Probing: a) sampling testing: no bad dice inking;
guaranteed good dice quantity≥93%.
b) 100% testing (if agreed with customer): wafer mapping data;
no bad dice inking.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5,5	V
Peak Pulse Power	P_{pp}	t_p=8/20us	80*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	4*	A
Electrostatic Discharge, all pins	V_{ESD}	IEC 61000-4-2, level 4. Contact.	±8	kV
Max.junction temperature	T_j	-	+125	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Reverse breakdown voltage. Pins 3, 4 to 2	I_R=1mA	6.1	7.0	8.5	V
I_R	Reverse leakage current. Pins 3, 4 to 2	V=+5V	-	-	0.8	uA
V_F	Forward voltage	I_F=1mA	-	-	0.9	V
V_{CL}	Clamping Voltage	I_{pp}=1A, t_p=8/20us I_{pp}=4A, t_p=8/20us	-	-	12* 20*	V
$C_{I/O}$	Pin capacitance. Pins 3, 4 to 2.	V_R=0V, f = 1 MHz	-	-	0.8	pF
$C_{I/O-I/O}$	Capacitance pin 3 to pin 4.	V_R=0V, f = 1 MHz	-	0.4	-	pF

*For Device testing.