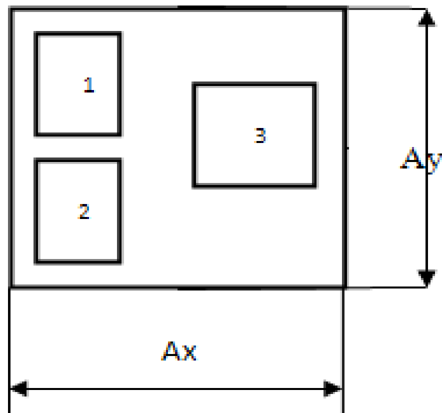

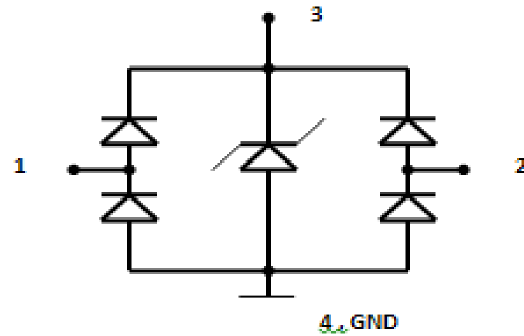

Mechanical data: A_x=380µm, A_y=420µm,

Schematic and pinning diagram

Pad size for Pin 1, 2 – 80*90µm
Pad size for Pin 3 – 140*100µm
Pin 4 – back side – GND
Chip thickness: a)138+/-12µm, b)470+/-20µm
Scribe Line width - 40µm
Top Metal: Al - for wire bonding
Backside: a)Ti-Ni-Ag for soldering, b)without metallization
Probing: 1) sampling testing – no bad dice inking, guaranteed good dice quantity≥93%
2) 100% testing (if agreed with customer) – wafer mapping data

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-Off Voltage	V_{RWM}	-	5	V
Peak pulse power - any I/O pin to Ground	P_{PP}	t_p= 8/20 µS	100**	W
Peak pulse current - any I/O pin to Ground	I_{PP}	t_p= 8/20 µS	4.0**	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4	>15 (air); >8 (contact)	kV
Max.junction temperature	T_j	-	+125*	°C

Characteristics (Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Breakdown Voltage	V_{BR}	IR=1mA, Pin3 to Pin4	6.1	7.0	8.5	V
Reverse leakage current	I_R	V=5V, Pin1,2,3 to Pin4 Pin3 to Pin1,2	-	-	0.9	µA
Forward voltage	V_F	I_F=15mA	-	-	1.15	V
Clamping Voltage – any I/O pin to Ground	V_{CL}	I_{PP}=1A, t_p=8/20µS; I_{PP}=4A, t_p=8/20µS	- -	- -	15** 25**	V
Capacitance – any I/O pin to Ground	C_j	V_R=0V; f=1MHz	-	-	0,8	pF
Capacitance – between I/O pins	C_j	V_R=0V; f=1MHz	-	-	0,4	pF

*- Tj=Ta+Rth(j-a)x(Pf+Pr), where Rth(j-a) – thermal resistance, Pf – forward power dissipation, Pr – revers power dissipation

** - For Device testing