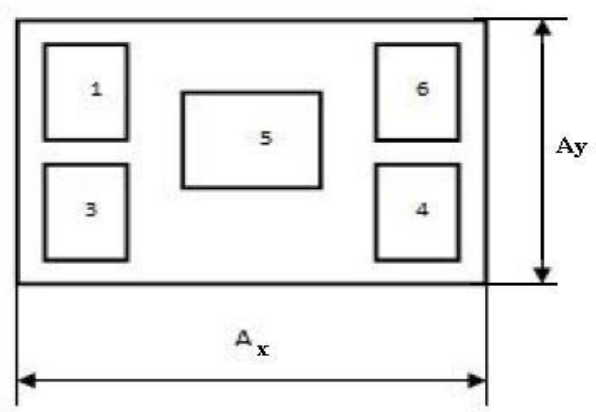
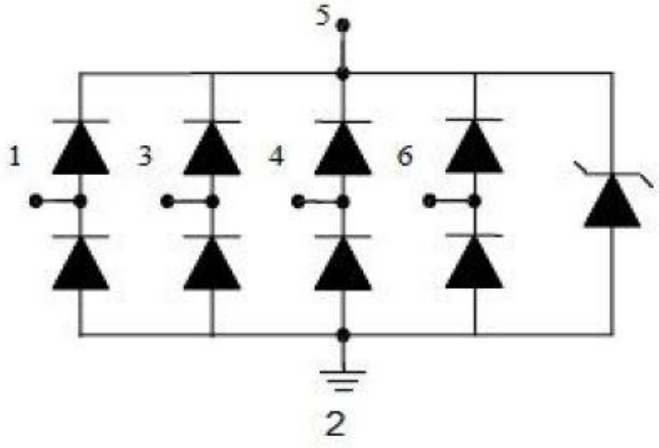
KSR-5.0V4M1

Ultra Low Capacitance TVS Diode





Pin 2 – back side – GND.

Mechanical date: A_x= 600 um, A_y=420um,
Pad Size for Pin 1, 3, 4, 6 - 85 *95 um.
Pad Size for Pin 5 -270*105 um.

Schematic and pinning diagram.

Chip thickness: a) 138+/-12um.
b) 470+/-20 um

Scribe Line width - 60um.

Top Metal: Al - for wire bonding

Back side - Anode: a) Ti-Ni-Ag for soldering
b) without metallization.

Probing:a) sampling testing: no bad dice inking guaranteed good dice quantity≥93%.
b) 100% testing (if agreed with customer): wafer mapping data
no bad dice inking

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	tp=8/20us	150**	W
Peak Pulse Current	I_{pp}	tp=8/20us	5**	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	Tj*	-	+150	ºC

Characteristics (Tj=25ºC)

PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Breakdown voltage	IR=1mA. Pin 5 to Pin 2.	6,1	8,0	8,5	V
Reverse leakage current	V=+5V. Pin 1, 3, 4, 5, 6 to Pin 2. V= - 5V. Pin 1, 3, 4, 6 to Pin 5.	-	-	0,9	uA
Forward voltage	IF=15mA. Pin 2 to Pin 1, 3, 4, 5, 6.	-	-	0,95	V
Clamping Voltage	Ipp=1.0A, tp=8/20us Pin 1, 3, 4, 6 to Pin 2.	-	-	15**	V
Clamping Voltage	Ipp=5.0A, tp=8/20us Pin 1, 3, 4, 6 to Pin 2.	-	-	28**	V
Capacitance. Any I/O pin to Ground	VR=0 V, f =1MHz	-		0,8	pF
Capacitance. Any I/O pin to I/O	VR=0 V, f =1MHz	-	-	0,4	pF

* Tj=Ta+Rth(j-a)x(Pf+Pr), where Rth(j-a) – thermal resistance, Pf – forward power dissipation, Pr – revers power dissipation
**For Device testing