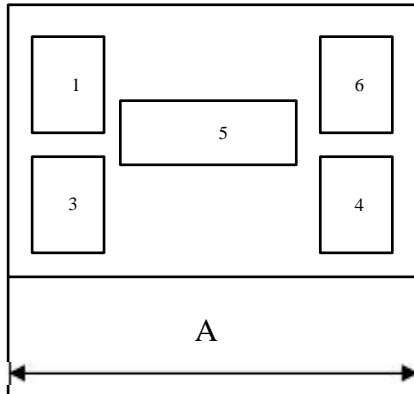


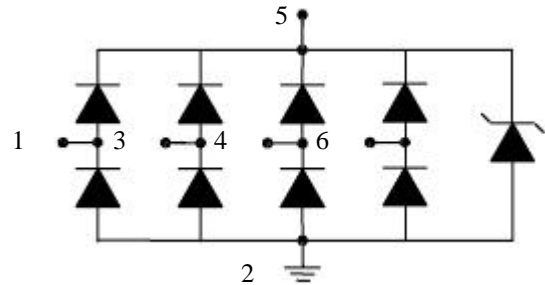
Specification. Rev. 1 Juli 2011. **KSR- 5.0V4M2.**

PRELIMINARY.

Low capacitance TVS Diode array.



Pin 2 – Back Side – GND.



Schematic and pinning diagram.

Mechanical date: $A_x= 800 \text{ um}$, $A_y=480\text{um}$,
Pad Size for Pin 1, 3, 4, 6 - $85 * 100 \text{ um}$.

Pad Size for Pin 5 - $250*160 \text{ um}$.

Chip thickness: $138\pm 12\text{um}$.

Scribe Line width - 60um .

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	$t_p=8/20\text{us}$	150*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\text{us}$	6*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	$I_R=1\text{mA}$	6,0	-	-	V
I_R	Reverse leakage current Pin 5 to 2	$V=5\text{V}$	-	-	3,0	μA
V_{CL}	Clamping Voltage Any I/O pin to pin 2	$I_{pp}=1.0\text{A}$, $t_p=8/20\text{us}$ $I_{pp}=6.0\text{A}$, $t_p=8/20\text{us}$	-	-	15* 25*	V
C_J	Capacitance. Any I/O pin to pin 2	$V_R=0 \text{ V}$, $f=1\text{MHz}$	-	-	3,0	pF

*- For Device testing