



Pin 2 – back side – GND

**Mechanical data:**  $A_x = 1000\mu\text{m}$ ,  $A_y = 780\mu\text{m}$

Pad Size for Pin 1, 3, 4, 6 -  $115 * 170 \mu\text{m}$ .

Pad Size for Pin 5 -  $115 * 100 \mu\text{m}$ .

**Chip thickness:**  $138 \pm 12 \mu\text{m}$ .

**Scribe Line width** -  $40 \mu\text{m}$ .

**Top Metal:** AlSi - for wire bonding.

**Back side:** Ti-Ni-Ag for soldering

**Probing:** 1) sampling testing: no bad dice inking guaranteed good dice quantity  $\geq 93\%$ .

2) 100% testing (if agreed with customer): bad dice inking;

**Schematic and pinning diagram**

### Limiting values

Parameter	Symbol	Conditions	Value	Unit
Peak pulse power	$P_{pp}$	8/20 uS pulse per diode	240*	W
Peak pulse current	$I_{pp}$	8/20 uS pulse per diode	12*	A
Electrostatic Discharge	ESD	IEC 61000-4-2, level 4 (ESD)	>15 (air); >15 (contact)	kV
Max.junction temperature	$T_j$		150	°C

### Characteristics ( $T_a = 25^\circ\text{C}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{RWM}$	Reverse Stand-Off Voltage. Pin 5 to 2.		-	-	5,0	V
$I_R$	Reverse leakage current. Pin 5 to 2.	$V_R = +5,0 \text{ V}$	-	-	5,0	$\mu\text{A}$
$V_{BR}$	Zener diode breakdown voltage. Pin 5 to 2.	$I_Z = 1 \text{ mA}$	5,8			V
$V_F$	Forward voltage	$I_F = 15 \text{ mA}$	-	-	1,15	V
$V_{CL}$	Clamping Voltage Pins 1, 3, 4, 6 to 2.	$I_{pp} = 1 \text{ A}$ , $t_{pp} = 8/20 \mu\text{S}$ ; $I_{pp} = 5 \text{ A}$ , $t_{pp} = 8/20 \mu\text{S}$ ; $I_{pp} = 12 \text{ A}$ , $t_{pp} = 8/20 \mu\text{S}$	-	-	10,0* 15,0* 20,0*	V
$C_{I/O}$	Capacitance to ground. (Pins 1, 3, 4, 6 to 2.)	$V_R = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ .	-	3,3	5,0	pF
$C_{I/O-I/O}$	Capacitance Between I/O pins.	$V_R = 0 \text{ V}$ ; $f = 1 \text{ MHz}$	-	1,5	-	pF

\*- For Device testing