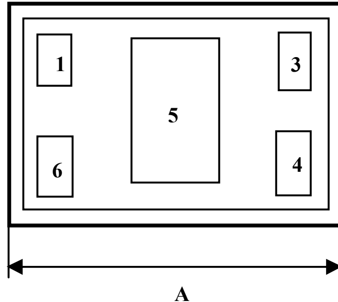
VSP-MIKRON

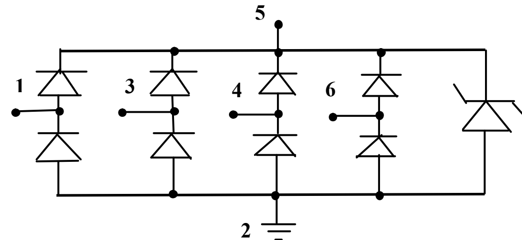
RoHS

Preliminary, March 2014

KSR-5,0V4

Low Capacitance TVS Diode Array in wafer form, 4 inch.





Schematic and pinning diagram.

Mechanical date: A_x=1020um; A_y=540um.
Thickness – 138+/-12um.
Scribe Line Width -60um.
Pin 1÷5 -Al metallization for wire bonding.
Pin 2 – Back side. Ti-Ni-Ag for soldering.
Probing: a) sampling testing: no bad dice inking;
guaranteed good dice quantity≥93%
b) 100% testing (if agreed with customer): wafer mapping data;
no bad dice inking.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Peak pulse power	P_{pp}	8/20 uS pulse per diode	300*	W
Peak pulse current	I_{pp}	8/20 uS pulse per diode	8,0*	A
Electrostatic Discharge	ESD	IEC 61000-4-2, level 4 (ESD)	>30 (air); >15 (contact)	kV
Max.junction temperature	T_j		150	ºC

Characteristics .Tj=25ºC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RWM}	Reverse Stand-Off Voltage. Pin 5 to 2.		-	-	5,0	V
I_R	Reverse leakage current. Pin 5 to 2.	V_R=+5,0 V		-	3,0	uA
V_{BR}	Zener diode breakdown voltage. Pin 5 to 2.	I_Z=1mA	6,1	7,0	8,5	V
V_F	Forward voltage	I_F=15mA	-	-	1,15	V
V_{CL}	Clamping Voltage Pins 1, 3, 4, 6 to 2.	I_{pp}=1A, t_{pp}=8/20uS; Ipp=5A, tpp=8/20uS	- -	12,5 -	14,0* 25,0*	V
$C_{I/O}$	Capacitance to ground. (Pins 1, 3, 4, 6 to 2.)	V_R=0 V; f = 1 MHz.	-	1,8	3,0	pF
$C_{I/O-I/O}$	Capacitance Between I/O pins.	Vr=0V; f=1MHz	-	0,9	-	pF

* - Preliminary. Only for Device testing.