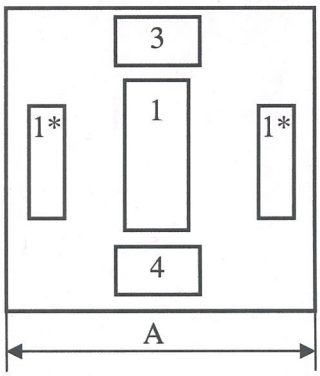
VSP-MIKRON

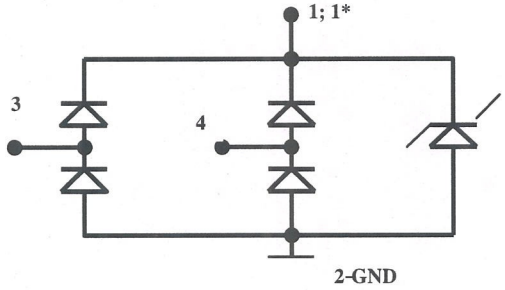
RoHS

KSR-XV2M1

Jan.2011

Chip for Low Capacitance 2-Line ESD protection.





Mechanical date: $A_x=A_y=1450$um.

Schematic and pinning diagram.

Pad Size: 1 – Ax=300um, Ay=620um;

1* - Ax=165um, Ay=540um; 3, 4 – Ax=395um, Ay=230um.

Die thickness – 138+/-12um

Scribe Line Width -60um.

Pin 1, 1*, 3, 4 -Al metallization for wire bond .

. Thickness Al – 4,0+/-0,4um.

Pin 2 – Back side. Metallization Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Peak Pulse Power	P_{pp}	t_p=2/10uS	2500*	W
Peak Pulse Current	I_{pp}	t_p=2/10uS	120*	A
Peak Pulse Current	I_{pp}	t_p=8/20uS	95*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4. Contact and Air.	±30,0	kV
Max.junction temperature	T_j		+125	°C

Characteristics .Tj=25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Reverse leakage current. Pins 3, 4 to ground	V=+5,0 V, T=25°C.	-	-	0,9	uA
I_R	Reverse leakage current. Pins 3, 4 to pin 1.	V= -5,0 V, T=25°C.	-	-	0,9	uA
V_{BR}	Reverse breakdown voltage. Pin 3,4 to ground.	I_R=1mA	6,1	-	-	V
V_F	Forward voltage . Pin 3, 4 to pin 1.	I_F=95A, t_p=8/20uS.	-	4,5*	-	V
V_F	Forward voltage . Pin 2 to pin 3, 4.	I_F=95A, t_p=8/20uS.	-	4,5*	-	V
$C_{I/O}$	Pin capacitance to ground. Pins 3, 4 to 2.	V_R=0 ; f = 1 MHz.	-	-	25	pF
$C_{I/O-I/O}$	Capacitance pin3 to pin4.	V_R=0 ; f = 1 MHz.	-	-	12	pF