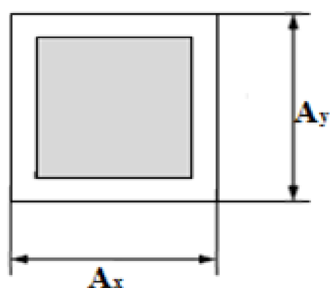

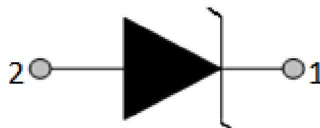

Schematic and pinning diagram

Mechanical date: A_x=A_y=330um
Bx=By=155um
Chip thickness: a) 630+/-20um on 6" wafer – SM-3.3L12
b) 138+/-12 on 4" wafer – SM-3.3L11
Scribe Line width - 50um.
Top Metal: AL with Ti under layer metallization for wire bond, thickness 2,2-2,4um.
Back side - Anode:a) without metallization – SM-3.3L12
b) Ti-Ni-Ag for soldering – SM-3.3L11
Top Side (Cathode) - pin 1, **Back Side (Anode)** - pin 2.
Sampling testing: no bad dice inking;
guaranteed good dice quantity≥95%.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	3,0	V
Peak Pulse Power	P_{pp}	t_p=8/20us	250*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	15*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>±15kV(Contact); >±15kV (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Ta=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=5mA	4,85	-	6,0	V
I_R	Reverse leakage current	V=3.0V	-	-	1,0	uA
V_F	Forward voltage	I_F=10mA	-	-	1,0	V
V_{CL}	Clamping Voltage	I_{pp}=1.0A, t_p=8/20us I_{pp}=15A, t_p=8/20us	-	-	6,7* 16,5*	V
C_J	Diode capacitance	V_R=0 V, f =1MHz	-	70	110	pF

*- For Device testing