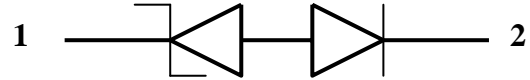
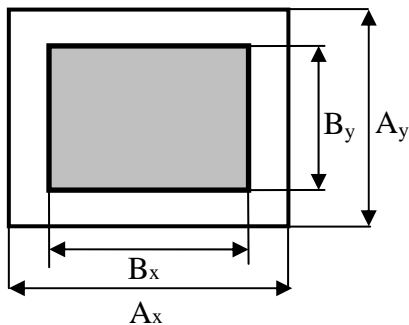


Rev.2. Jan. 2011.

SM-3,3V2
Chip TVS diode for TVS array TClamp3302.


Mechanical date: $A_x=1450\mu\text{m}$, $A_y=580\mu\text{m}$.
 $B_x=1270\mu\text{m}$, $B_y=400\mu\text{m}$

Schematic and pinning diagram.

Chip thickness: $138\pm 12\mu\text{m}$

Scribe Line width - $60\mu\text{m}$.

Top Metal: Al - for wire bonding, $d=4.0\pm 0.2\mu\text{m}$.

Back side: Ti-Ni-Ag for soldering.

Top Side - pin 1 – Cathode, **Back Side** - pin 2.–Anode

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Working Peak Reverse Voltage	V_{RWM}		3,3	V
Peak Pulse Power	P_{pp}	$t_p= 2/10\mu\text{s}$	2500*	W
Max. Peak Pulse Current	I_{pp}	$t_p= 2/10\mu\text{s}$	120*	A
Max. Peak Pulse Current	I_{PP}	$t_p= 8/20\mu\text{s}$	95,0*	A
Electrostatic discharge	V_{ESD}	IEC 61000-4-2. Level-4.	+/-30,0 –Contact. +/-30,0 – Air.	kV
Max.Junction Temperature	T_j	-	+125	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Diode reverse leakage current.	$V_R=3,3\text{V}$; $T=25^\circ\text{C}$. “+” on pin 1.	-	-	0,9	μA
V_{PT}	Punch-Through Voltage.	$I_{PT}=2\mu\text{A}$; $T=25^\circ\text{C}$.	3,5	-	-	V
V_{SB}	Snap-Back Voltage	$I_{SB}=50\text{mA}$	2,8	-	-	V
C_j	Diode capacitance .	$F=1\text{MHz}$, $V_{dc}=0\text{V}$.	-	250	-	pF
V_{CL}	Clamping voltage	$I_R=100\text{A}$, $t_p=2/10\mu\text{s}$	-	-	19,0*	V

*- For Device testing.