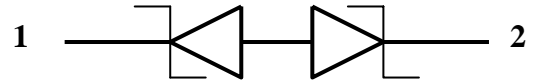
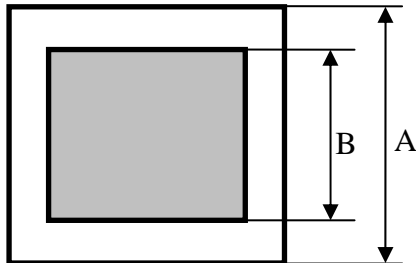


SMB-05L41, SMB-05L42

Chip Bi - directional TVS diode.



Mechanical date: $A_x=A_y=280\mu\text{m}$, $B_x= B_y= 100\mu\text{m}$

Chip thickness: a) $138\pm 12\mu\text{m}$ – for SMB-05L41;

b) $470\pm 20\mu\text{m}$ – for SMB-05L42.

Scribe Line width - 60 μm .

Top Metal: Al - for wire bonding, $d=2.2\pm 0.2 \mu\text{m}$.

Back side: a) Ti-Ni-Ag for Soldering – for SMB-05L41;

b) not to make grinding, without metallization – for SMB-05L42.

Top Side - pin 1, **Back Side** - pin 2.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	$t_p=8/20\mu\text{s}$	45*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{s}$	3,5*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	+/-8 (Contact); +/-15 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage. Pin 1 to 2.	$I_R=50\text{mA}$	5.3	-	7.5	V
I_R	Reverse leakage current.	$V=\pm 5\text{V}$		-	90	nA
V_{CL}	Clamping Voltage	$I_{pp}=1\text{A}$, $t_p=8/20\mu\text{s}$ $I_{pp}=3.5\text{A}$, $t_p=8/20\mu\text{s}$	-	-	9.0* 12.5*	V
C_J	Diode capacitance. Pin 1 to 2.	$V_R=0 \text{V}$, $f=1\text{MHz}$	-	5.0	6.0	pF

*- For Device testing.