



**Mechanical data:**  $A_x=A_y=280\mu\text{m}$

**Chip thickness:**  $635 \pm 20\mu\text{m}$

**Scribe Line width** -  $45\mu\text{m}$ .

**Top Metal:** Ti-Ni-Ag for Soldering.

**Back side** : without metallization

**Top Side** - pin 1, **Back Side** - pin 2.

**Probing: sampling testing:** no bad dice inking, guaranteed good dice quantity  $\geq 95\%$ .

**Schematic and pinning diagram**

### Limiting values

Parameter	Symbol	Conditions	Value	Unit
Working Peak Reverse Voltage	$V_{RWM}$		5,0.	V
Peak Pulse Power	$P_{pp}$	$t_p= 8/20\mu\text{s}$	85*	W
Peak Pulse Current	$I_{pp}$	$t_p= 8/20\mu\text{s}$	5,0*	A
Electrostatic Discharge	$V_{ESD}$	IEC 61000-4-2, level 4.	+/-18,0 (Contact); +/-18,0 (Air).	kV
Max.junction temperature	$T_j$		+150	$^{\circ}\text{C}$

### Characteristics ( $T_a=25^{\circ}\text{C}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_R$	Diode reverse leakage current.	$V=\pm 5\text{ V}$	-	-	100	nA
$V_{BR}$	Breakdown voltage. Pin1 to 2 and Pin 2 to 1	$I_R=1\text{ mA}$	5,6	-	9,4	V
$C_j$	Diode capacitance .	$f=1\text{ MHz}, V_{dc}=0\text{ V}.$	8,0	10	13,0	pF
$V_{CL}$	Clamping Voltage	$I_{pp}=1,0\text{ A};$ $I_{pp}= 5,0\text{ A};$ $t_p= 8/20\mu\text{ s} .$	-	-	9,0* 17,0*	V

\*- For Device testing