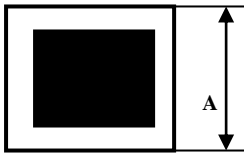


## SMB-05L51, SMB-05L52

Chip Bi- directional TVS diode in wafer form, 4 inch. Die size: 8\*8mil.



**Mechanical data:**  $A_x=210\mu\text{m}$ .  $A_y=210\mu\text{m}$ .

**Chip thickness:** a)  $138\pm 12\mu\text{m}$  – for SMB-05L51;

b) without grinding  $470\pm 20\mu\text{m}$  – for SMB-05L52.

**Top Metal:** Al- for wire bonding.

**Back side:** a) Ti-Ni-Ag for Soldering – for SMB-05L51

b) without metallization – for SMB-05L52

**Scribe Line Width** –  $40\mu\text{m}$ .

**Sampling testing:** no bad dice inking;  
guaranteed good dice quantity  $\geq 95\%$ .

### Limiting values

Parameter	Symbol	Conditions	Value	Unit
Working Peak Reverse Voltage	$V_{RWM}$		5,0.	V
Peak Pulse Power	$P_{pp}$	$t_p=8/20\mu\text{S}$	35*	W
Peak Pulse Current	$I_{pp}$	$t_p=8/20\mu\text{S}$	2,0*	A
Electrostatic Discharge	$V_{ESD}$	IEC 61000-4-2, level 4.	+/-8,0 (Contact); +/-15,0 (Air).	kV
Max.junction temperature	$T_j$		+150	°C

### Characteristics . $T_j=25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_R$	Diode reverse leakage current.	$V=\pm 5,0\text{ V}$	-	-	90	nA
$V_{BR}$	Breakdown voltage. Pin 1 to 2 or Pin2 to 1.	$I_R=1\text{mA}$	5,6	-	9,4	V
$C_j$	Diode capacitance .	$F=1\text{MHz}$ , $V_{dc}=0\text{ V}$ .	-	3,0	3,5	pF
$V_{CL}$	lamping voltage	$I_{pp}=1,0\text{A}$ ; $I_{pp}=2,0\text{A}$ ; $t_p=8/20\mu\text{S}$ .	-	-	10,0* 13,0*	V

\*For Device testing.