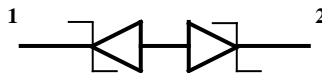
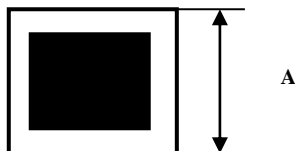




SMB-3,3L33; SMB-3,3L34.

Chip Bi- directional TVS diode



Mechanical data: $A_x=380\mu\text{m}$. $A_y=380\mu\text{m}$.

Chip thickness: a) $138\pm 12\mu\text{m}$ – for SMB-3,3L33;

b) $470\pm 20\mu\text{m}$ – for SMB-3,3L34.

Top Metal: Al- for wire bonding.

Back side: a) SMB-3.3L33 - Ti-Ni-Ag for Soldering.;

b) SMB-3.3L34 – without metallization.

Probing: a) **sampling testing:** no bad dice inking;

guaranteed good dice quantity $\geq 95\%$.

b) **100% testing (if agreed with customer):** wafer mapping data;

no bad dice inking.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Working Peak Reverse Voltage	V_{RWM}	-	3,3	V
Peak Pulse Power	P_{pp}	$t_p=8/20\mu\text{S}$	250*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{S}$	15,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	+/-10,0 (Contact); +/-25,0 (Air).	kV
Max.junction temperature	T_j		+150	°C

Characteristics . $T_j=25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Diode reverse leakage current.	$V=\pm 3,0\text{ V}$	-	0,05	0,9	μA
V_{BR}	Breakdown voltage. Pin 1 to 2 & Pin 2 to 1	$I_R=1\text{mA}$	3,5	-	-	V
V_{PT}	Punch-Through Voltage	$I_{PT}=2\mu\text{A}$	3,5	-	-	V
V_{sb}	Snap-Back Voltage	$I_{sb}=50\text{mA}$	3,3	-	5,3	V
C_j	Diode capacitance .	$f=1\text{MHz}$, $V_{dc}=0\text{ V}$.	-	25		pF
V_{CL}	Clamping voltage	$I_{pp}=1,0\text{A}$; $I_{pp}=15,0\text{A}$; $t_p=8/20\mu\text{S}$.	-	-	5,5* 10,0*	V

*For Device testing.